31.8 A 0.36W 6b up to 20GS/s DAC for UWB Wave Formation

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A number of waveforms are used for UWB transmission [1], including Gaussian-pulse derivatives, tri-wave, and Gaussian-enveloped radio pulse. A method is required that permits the dynamic and adaptive creation of impulses, a key to ensure UWB system interoperability at the physical layer. The method presented in this paper is to utilize DAC-based direct waveform synthesis (DWS).

6b DAC is found to be sufficient for the task. The usage of the UWB frequency spectrum (3.1 to 10.6GHz) below 5GHz requires ~8GS/s, while ~16GS/s is needed for the upper band. Additionally, low-power operation is essential for handheld devices.

Each data bit in the DAC originates at the output of a MUX with equivalent driving capability and then passes to the current switch (CS) through a driver (DRV) (Fig. 31.8.1). The challenge is to equalize the delays between data bits that steer currents differing in a 1:32 range. LSB is formed not by halving the current, but by applying it into a 25Ω portion of the on-chip 50Ω load resistor. This reduces the current range to 1:16. Scaled drivers are used to reduce the range down to 1:4 at the outputs of the MUX. The larger parasitic capacitance of the DRV loading the MUX output causes delay; there is also more delay on the input of CSs of more significant bits. The difference in delays is reduced by scaling the emitter length of the transistors used in the DRV and CS instead of using parallel connections of the same power cells. Final equalization of the delays is achieved by adjusting delays tc_1, …, tc_6 at the output of the clock drivers. More significant bits have their retiming moment earlier with respect to less significant bits. 4ps worst-case misalignment is achieved in simulation.

CS transistor base shunts part of the emitter current and reduces the accuracy of the voltage step on the load resistor (Fig. 31.8.2). A base current compensation circuitry is used. Current mirror CM1 doubles the base current and inserts it back to the reference current that is already short of one base current. When the base current is subtracted in the current switch, its collector current is equal to reference. The load resistor consists of a parallel combination of internal and external 50Ω resistors. On-chip resistors vary over process corners and temperature, so a reference current is formed as a 50/50 combination of current produced using internal and external resistors. Combining currents with positive and negative temperature coefficients ensures stability over temperature.

The power supply voltage of CML circuits can be reduced from about 2.5V down to 1.5V by changing the circuit architecture from dual-level to single-level [2]; however, there is no power savings, as the current in the circuit doubles. A new approach in operating the two-level CML circuits is developed to enable V_{CC}=1.8V. The minimum power supply for the typical CML circuit is limited by the sum of voltages: $V_{sat3}+V_{sat2}+V_{sw}/2$ (from the lower side) and $V_{be1}+V_{sw}/2$ (from the upper side) (Fig. 31.8.3). According to simulations V_{sat}=0.28V and V_{be}=0.95V at -25˚C and V_{sat}=0.32V and V_{be}=0.78V at 125˚C (worst case process [3] corners). At –25˚C it yields: $V_{CCmin}=2\times V_{sat}+V_{be}+V_{sw}$=1.62V ($V_{sw}$=0.11V). At 125˚C it is also 1.62V (V_{sw}=0.2V). At V_{CC}=1.7V, 78mV flexibility in setting the bias makes the circuit implementation feasible.

Data is retimed using a half clock rate at the output of the 4:1 MUX (Fig. 31.8.4). 4:1 MUXes reduce the line rate of incoming data by a factor of 4. The 6×20Gb/s input data stream needed for the 6b DAC is transformed into a 24×5Gb/s data stream, which is easier to produce though still too high for performance testing and chip screening. Thus, a BIST function is implemented to generate a predetermined waveform for quick assessment of the DAC operation without applying incoming data. A 2:1 MUX routes either incoming or predefined data from the ROM to the DAC. Data from the memory is MUXed up by 4 so that it can be handled at a lower data rate to further reduce the power.

The chip size is 2.5×2.5mm^2 (Fig. 31.8.7). There are 6 metals used for interconnects; the top metal (the thickest) is used to form the ground plane. The DAC core occupies 0.5% of the chip area. The rest of the chip area is used for 4:1 MUX, BIST, data and clock input buffers, biasing and control functions, as well as reference voltage and power-supply bypassing capacitors. A 104-lead QFN package is used. The discontinuity introduced by the inductive behavior of the bonding wires (~2mm long) is expected to compromise the performance.

It is difficult to form 24×5Gb/s data needed for chip testing at 20GS/s, so the BIST mode is used to verify the maximum data rate of the DAC. A waveform of 6b at 16 samples is programmed in the ROM (Fig. 31.8.5). The measured waveform matches the simulated waveform well and matches the ideal waveform fairly well (Fig. 31.8.5).

A bank of six Xilinx Virtex II Pro FPGAs is used to produce the datastream needed for UWB pulse formation. However, line-rate speed in this case is limited by the FPGA and is found to be about 3.75Gb/s. This limits the DAC sampling rate to 15GS/s. A 185.8MHz coherent sampled sinusoidal is synthesized for SFDR measurement (Fig. 31.8.5). As follows from the measured spectrum, SFDR is 50dBc. SFDR is expected to decrease with increasing of the frequency of the synthesized signal. First and second derivatives of Gaussian pulse are also synthesized at Nyquist sampling rate (Fig. 31.8.6). DWS also produces bi-phase modulated tri-wave and Gaussian-enveloped radio pulses (Fig. 31.8.6). Synthesizing waveforms at full-and half-Nyquist rate at 15GS/s enables splitting of the UWB spectrum into two bands. Deviations from ideal forms are caused by reflections due to discontinuities in DAC socket, chip wire-bonds, and SMA connector.

As demonstrated, DAC enables the direct formation of a number of modulated waveforms for use in UWB communications. The optimized architecture of the DAC in combination with the new approach for biasing of the two-level CML circuits allows for reduction of the power supply voltage down to 1.8V and subsequently power dissipation to 0.36W. FOM of the DAC defined as: $FOM=Power/(2^N\times SampleRate)$, yields to 0.28pJ. A DAC with a similar performance presented in [4] has 0.72pJ FOM. Therefore, the DAC presented here has 2.57 times better FOM despite using 0.18μm SiGe process as opposed to 0.13μm used in [4].

Acknowledgements:
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References:
[1] R. Sengottaiyan, "Circuit Techniques for Dual-band UWB Wireless Communication," *ISSCC Dig. Tech. Papers*, pp. 656-660, Feb., 2004.
[2] B. Razavi, "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 332-339, Mar., 1994.
[3] M. Racanelli, P. Kempf, "SiGe BiCMOS Technology for RF Circuit Applications," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1259-1270, July, 2005.
[4] P. Schvan et al., "A 22GS/s 6b DAC with Integrated Digital Ramp Generator," *ISSCC Dig. Tech. Papers*, pp. 122-123, Feb., 2005.

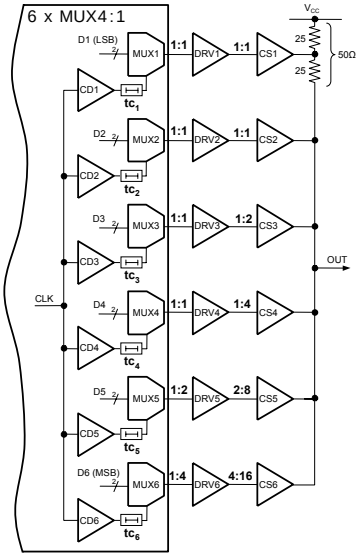

Figure 31.8.1: DAC back-end block diagram.

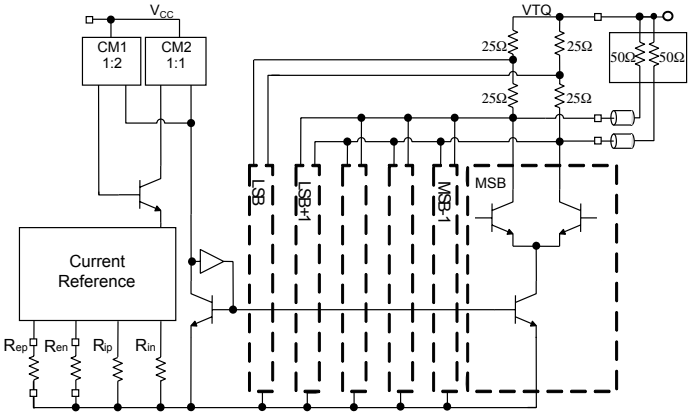

Figure 31.8.2: Simplified schematic of the DAC.

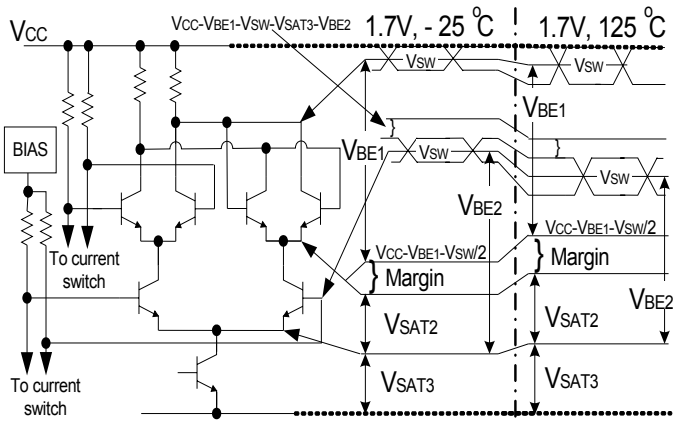

Figure 31.8.3: Low-voltage bias of CML circuits.

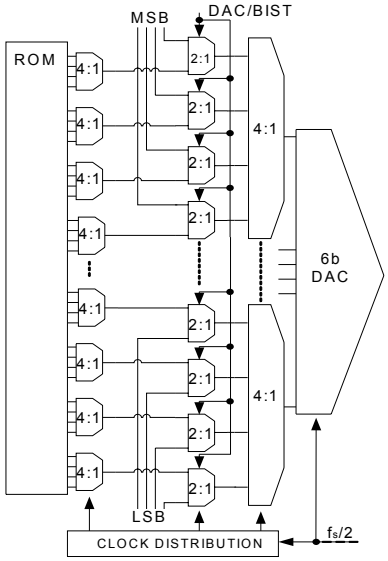

Figure 31.8.4: Block diagram of the data path.

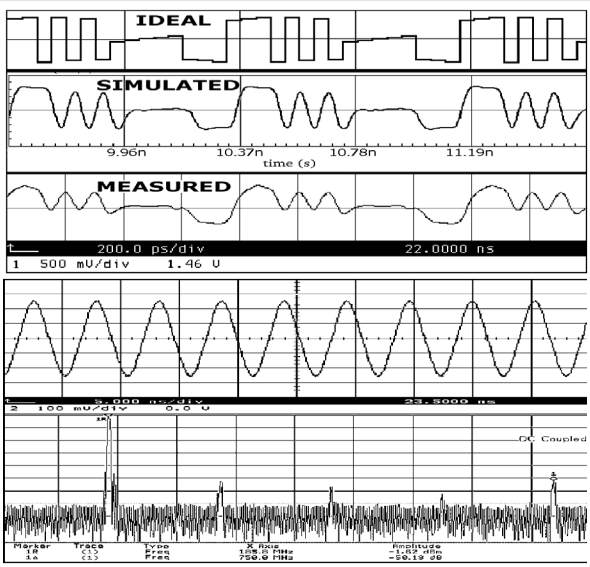

Figure 31.8.5: Waveforms for self-test and SFDR measurement.

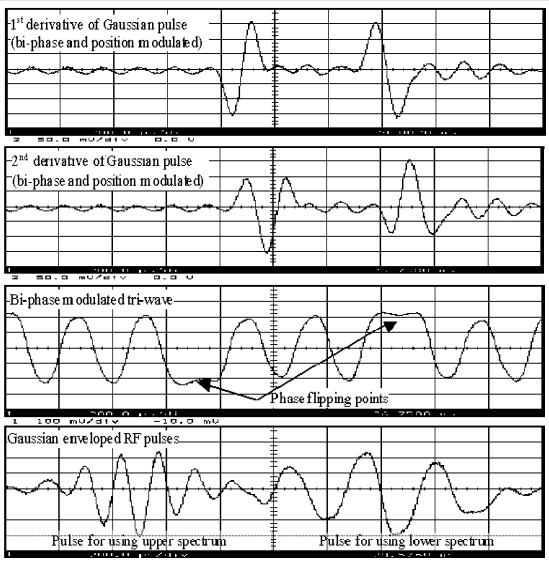

Figure 31.8.6: Synthesized UWB pulses.

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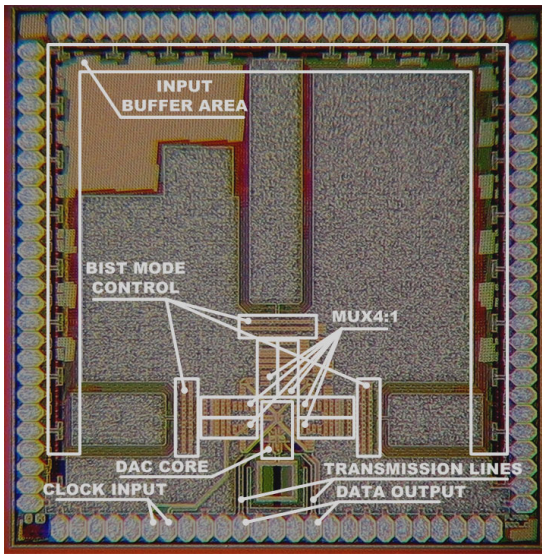

Figure 31.8.7: Chip micrograph.

